This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of state "0", state "1", state "2", and state "3" of data that differ in threshold voltage;

a data storage circuit which is connected to said bit line and stores not only data of a first or a second logical level externally supplied but also the data of the first or second level read from said memory element; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said data storage circuit, wherein

said control circuit operates in such a manner that

in a first operation, the control circuit changes the data in said memory element from said state "0" to state "1" when the data in said data storage circuit is data of the first logical level and keeps the data in said memory element in said state "0" when the data in said data storage circuit is data of the second logical level,

that in a first verify operation of verifying whether said data has reached state "1", the control circuit brings the data in said data storage circuit to the second logical level when the data in said data storage circuit is at the first logical level and said data has reached state "1", keeps the data in said data storage circuit at the first logical level when said data has not reached state "1", keeps the data in said data storage circuit at the second logical level when the data in said data storage circuit is at the second logical level, and carries out said first operation until the data in said data storage circuit has reached the second logical level, and

that in a second operation, the control circuit changes the data in said memory element from state "1" to state "2" when the data in said data storage circuit is data of the first logical level externally supplied and the data in said memory element is in state "1", and changes the data in said memory element from state "0" to state "3", when the data in said memory element is in state "0".

2. The nonvolatile semiconductor memory device according to claim 1, wherein

said control circuit, in a second verify operation of verifying whether the data in said memory element has reached state "2", brings the data in said data storage circuit to the second logical level when the data has reached state "2" in a case where the data in said data storage circuit is at the first logical level and the data in said memory element is in state "1" before said second operation is carried out, keeps the data in said data storage circuit at the first logical level when the data has not reached state "2", prevents the logical level in said data storage circuit from changing when the data in said memory element is in state "0" before said second operation is carried out, and keeps the data in said data storage circuit at the second logical level when the data in said data storage circuit is at the second logical level, and furthermore

said control circuit, in a third verify operation of verifying whether the data in said memory element has reached state "3", brings the data in said data storage circuit to the second logical level when the data in said data storage circuit is at the first logical level and the data has reached state "3", keeps the data in said data storage circuit at the first logical level when the data has not reached state "3", keeps the data in said data storage circuit at the second memory logical level when the data in said data storage circuit is at the second logical level, and carries out said second operation, second and third verify operations until the data in said data storage circuit has reached the second logical level.

3. The nonvolatile semiconductor memory device according to claim 1, wherein

said control circuit, in said second operation, omits the verify operation of verifying whether said data has reached state "3" in the first half of the verify operation of verifying

whether said data has reached state "2" and omits the verify operation of verifying whether said data has reached state "2" in the latter half of the verify operation of verifying whether said data h as reached state "3".

4. The nonvolatile semiconductor memory device according to claim 1, wherein

said control circuit sets an initial write voltage in changing the data in said memory element from state "0" to state "3" and in changing the data from state "1" to state "2" higher than an initial write voltage in changing the data in said memory element from state "0" to state "1".

5. The nonvolatile semiconductor memory device according to claim 1, wherein

said control circuit, judges whether the data in said memory element is in either state "2" or below or state "3" when the data in said memory element is read, stores the result of the judgment in said data storage circuit, thereafter judges whether the data is in either state "0" or state "1" or above, and, if the data stored in said data storage circuit is in state "3", brings the potential on the bit line connected to the memory element in which the data has been stored to a low level and keeps the potential of the bit lines connected to the memory elements whose data is in either state "1" or state "2" at a high level.

6. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and store s one of state "0", state "1", state "2", and state "3" of data that differ in threshold voltage;

a first storage circuit which is connected to said bit line and stores data of a first or a second logical level externally supplied;

a second storage circuit which is connected to said bit line and stores the data of the first or second level read from said memory element; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said first and second storage circuits, wherein

said control circuit operates in such a manner that

in a first operation, the control circuit changes the data in said memory element from state "0" to state "1" when the data in said first data storage circuit is data of the first logical level and keeps the data in said memory element at said state "0" when the data in said first storage circuit is data of the second logical level,

that in a first verify operation of verifying whether said data has reached state "1", the control circuit brings the data in said first storage circuit to the second logical level when the data in said first storage circuit is at the first logical level and said data has reached state "1", keeps the data in said first storage circuit at the first logical level when said data has not reached state "1", keeps the data in said first storage circuit at the second logical level when the data in said first storage circuit is at the second logical level, and carries out said first operation until the data in said first storage circuit has reached the second logical level,

that in a second operation, the control circuit stores the data read from said memory element into said second storage circuit, changes the data in said memory element from state "1" to state "2" when the data in said first storage circuit is data of the first logical level externally supplied, changes the data in said memory element from state "0" to state "3" when the data in said memory element is in state "0", and keeps the data in said memory element when the data in said first storage circuit is data of the second logical level,

that in a second verify operation of verifying whether the data in said memory element has reached state "2", the control circuit brings the data in said first storage circuit to the second logical level when the data has reached state "2" in a case where the data in said first storage circuit is at the first logical level and the data in said memory element is in state "1" before the second operation is carried out, keeps the data in said first storage circuit at the first logical level when said data has not reached state "2", and brings the potential on the bit line to which the

memory element is connected to the first logical level and the data in said first storage circuit to the first logical level when the data in said second storage circuit is at the second logical level in a case where the data in said memory element is in state "0" before said second operation is carried out, and

that in a third verify operation of verifying said data has reached state "3", the control circuit brings the data in said first storage circuit to the second logical level when the data in said first storage circuit is at the first logical level and said data has reached state "3", keeps the data in said first storage circuit at the first logical level when said data has not reached state "3", keeps the data in said first storage circuit at the second memory logical level when the data in said first storage circuit is at the second logical level, and carries out said second operation and second and third verify operations until the data in said first storage circuit has reached the second logical level.

7. The nonvolatile semiconductor memory device according to claim 6, wherein

said control circuit, in said second operation, omits the verify operation of verifying whether said data has reached state "3" in the first half of the verify operation of verifying whether said data has reached state "2" and omits the verify operation of verifying whether said data has reached state "2" in the latter half of the verify operation of verifying whether said data has reached state "3".

8. The nonvolatile semiconductor memory device according to claim 6, wherein

said control circuit sets an initial write voltage in changing the data in said memory element from state "0" to state "3" and in changing the data from state "1" to state "2" higher than an initial write voltage in changing the data in said memory element from state "0" to state "1".

9. The nonvolatile semiconductor memory device according to claim 6, wherein

said control circuit, judges whether the data in said memory element is in either state "2" or below or state "3" when the data in said memory element is read, stores the result of the judgment in said data storage circuit, thereafter judges whether the data is in either state "0" or state "1" or above, and, if the data stored in said data storage circuit is in state "3", brings the potential on the bit line connected to the memory element in which the data has been stored to a low level and keeps the potential of the bit lines connected to the memory elements whose data is in either state "1" or state "2" at a high level.

10. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of an n number of data items made up of state "0", state "1", . . . , state "n" ($3 \leq n$ where n is a natural number);

a data storage circuit which stores data of a first or a second logical level externally inputted; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said data storage circuit, wherein

said control circuit, in a final write operation, charges state "0" of the smallest data stored in said memory element into state "n" of the largest data when the data in said first storage circuit is data of the first logical level externally supplied, and keeps the data in said memory element when the data in said first storage circuit is data of the second logical level.

11. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit, in a second verify operation of verifying whether the data in said memory element has reached state "2", charges the data in said data storage circuit to the second logical level when the data has reached state "2", in a case where the data in said data storage circuit is at the first logical level and the data in said memory element is in state "1" before said

second operation is carried out, keeps the data in said data storage circuit at the first logical level when the data has not reached state "2", prevents the logical level in said data storage circuit from changing when the data in said memory element is in state "0" before said second operation is carried out, and keeps the data in said data storage circuit at the second logical level when the data in said data storage circuit is at the second logical level, and furthermore

said control circuit, in a third verify operation of verifying whether the data in said memory element has reached state "3", charges the data in said data storage circuit to the second logical level when the data in said data storage circuit is at the first logical level and the data has reached state "3", keeps the data in said data storage circuit at the first logical level when the data has not reached state "3", keeps the data in said data storage circuit at the second memory logical level when the data in said data storage circuit is at the second logical level, and carries out said second operation, second and third verify operations until the data in said data storage circuit has reached the second logical level.

12. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit, judges whether the data in said memory element is in either state "2" or below or state "3" when the data in said memory element is read, stores the result of the judgment in said data storage circuit, thereafter judges whether the data is in either state "0" or state "1" or above, and, if the data stored in said data storage circuit is in state "3", charges the potential on the bit line connected to the memory element in which the data has been stored to a low level and keeps the potential of the bit lines connected to the memory elements whose data is in either state "1" or state "2" at a high level.

13. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit, in said second operation, omits the verify operation of verifying whether said data has reached state "3" in the first half of the verify operation of verifying whether said data has reached state "2" and omits the verify operation of verifying whether said

data has reached state "2" in the latter half of the verify operation of verifying whether said data has reached state "3".

14. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit sets an initial write voltage in changing the data in said memory element from state "0" to state "3" and in changing the data from state "1" to state "2" higher than an initial write voltage in changing the data in said memory element from state "0" to state "3".

15. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of state "0", state "1", state "2", and state "3" of data that differ in threshold voltage;

a data storage circuit which is connected to said bit line and stores the data read from said memory element; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said data storage circuit, wherein

said control circuit operates in such a manner that

in a first read operation, the control circuit sets data of a first logical level in said data storage circuit when the data in said memory element is in either state "0" or state "1", and sets data of a second logical level in said data storage circuit when the data in said memory element is in either state "2" or state "3", and

that in a second read operation, the control circuit sets data of the first logical level in said data storage circuit when the data in said memory element is in either state "0" or state "3", and sets data of the second logical level in said data storage circuit when the data in said memory element is in either state "1" or state "2".

16. The nonvolatile semiconductor memory device according to claim 15, wherein

said control circuit judges whether the data in said memory element is in either state "1" or below or state "2" or above in said first read operation and judges not only whether the data in said memory element is in either state "0" or state "1" or above but also whether the data is in either state "2" or below or state "3" in said second read operation.

Add claim 17 as follows:

17. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of state "0", state "1", state "2", and state "3" of data that differ in threshold voltage;

a control circuit which controls a potential on said bit line and that on said word line, wherein

said control circuit operates in such a manner that

in a first read operation, the bit line receives data of a first logical level when the data in said memory element is in either state "0" or state "1", and receives data a second logical level when the data in said memory element is in either state "2" or state "3", and

that in a second read operation, the bit line receives data of the first logical level when the data in said memory element is in either state "0" or state "3", and receives data of the second logical level when the data in said memory element is in either state "1" or state "2".

Add claim 18 as follows:

18. The nonvolatile semiconductor memory device according to claim 15, wherein

said control circuit judges whether the data in said memory element is in either state "1" or below or state "2" or above in said first read operation and judges not only whether the data in said memory element is in either state "0" or state "1" or above but also whether the data is in either state "2" or below or state "3" in said second read operation.

Add claim 19 as follows:

19. A semiconductor memory device comprising:

a nonvolatile memory cell array having bit lines and word lines;

a plurality of memory cell transistors, commonly connected to one of the word lines, forming a physical row to store data for first and second addressable pages; and

a control voltage generator configured to generate reading voltages to be applied to the word lines, wherein

in a first read operation, the control voltage generator generates a single reference voltage to sense data of the second addressable page, and in a second read operation, the control voltage generator generates only two reference voltages to sense data of the first addressable page.

Add claim 20 as follows:

20. The semiconductor memory device according to claim 19, wherein

the nonvolatile memory cell array includes a plurality of memory cell transistor strings, each of the strings including serially connected memory cell transistors and select gate transistors.

Add claim 21 as follows:

21. The semiconductor memory device according to claim 20, further comprising:

a data storage circuit connected to the bit lines;

an I/O buffer connected to the data storage circuit; and

an input/output terminal connected to the I/O buffer circuit.

Add claim 22 as follows:

22. The semiconductor memory device according to claim 19, wherein the second read operation only senses the values of the nonvolatile memory cell array based on at least one of the two reference voltages.

Add claim 23 as follows:

23. A semiconductor memory device comprising:

at least one memory array with word lines and bit lines, said memory array storing multivalued data in memory cells, said multivalued data including at least a first page and a second page of data;

at least one control circuit connected to said at least one memory array,

wherein said at least one control circuit reads one of said first page of data and said second page of data for a first set of said memory cells and then reads the same one of said first page of data and said second page of data for a second set of memory cells.

Add claim 24 as follows:

24. The semiconductor memory device according to claim 23, wherein a first page of data is read followed by another first page of data.

Add claim 25 as follows:

25. The semiconductor memory device according to claim 23, wherein a second page of data is read followed by another second page of data.

Add claim 26 as follows:

26. The semiconductor memory device according to claim 23, further comprising:

data storage circuits for receiving one of said first page of data and said second page of data.

Add claim 27 as follows:

27. The semiconductor memory device according to claim 23, further comprising:

at least one input/output buffer connected to the data storage circuit; and

an input/output terminal connected to the input/output buffer circuit.

Add claim 28 as follows:

28. A semiconductor memory device comprising:

at least one memory array with word lines and bit lines, said memory array storing multivalued data in memory cells, said multivalued data including at least a first page, a second page of data, and a third page of data;

at least one control circuit connected to said at least one memory array,

wherein said at least one control circuit reads one of said first page, said second page, and said third page of data and then reads the same one of said first page, said second page, and said third page of data for a second set of memory cells.

Add claim 29 as follows:

29. A semiconductor memory device comprising:

a memory cell array having bit lines and word lines, said memory cell array storing multilevel data in at least a first page and a second page of data wherein said first page and said second page of data are distinguished by threshold voltages;

a control circuit connected to said memory cell array for controlling potentials applied at least to one of said word lines,

wherein a potential applied to said one of said word lines has a first value for reading one of said first page and said second page of data from memory cells and has no more than two values for reading the other of said first page and said second page of data.

Add claim 30 as follows:

30. The semiconductor memory device of claim 29, further comprising:

a data storage circuit receiving said one of said first page and said second page of data and then receiving said other of said first page and said second page of data.

Add claim 31 as follows:

31. The semiconductor memory device of claim 30, wherein said data storage circuit is controlled by said control circuit.

Add claim 32 as follows:

32. The semiconductor memory device of claim 29, wherein said control circuit controls said potentials during a read operation.

Add claim 33 as follows:

33. The semiconductor memory device of claim 29, wherein said control circuit controls said potentials during a verify operation.

Add claim 34 as follows:

34. The semiconductor memory device of claim 29, wherein said control circuit controls said potentials during a read operation and during a verify operation.

Add claim 35 as follows:

35. The semiconductor memory device of claim 29, wherein said control circuit controls the potentials on said word line as between 0 V and 0.3 V, 0.5 V and 0.8 V, and 1.0 V and 1.3V for potential values applied to said word lines.

Add claim 36 as follows:

36. The semiconductor memory device of claim 29, wherein threshold voltages for memory cells in said memory cell array have at least the following four value ranges:

0 V or below,

0.3 V to 0.5 V,

0.8 V to 1.0 V,

1.3 V to 1.5 V.

Add claim 37 as follows:

37. The semiconductor memory device of claim 30, wherein said data storage circuit comprises a sense amplifier.

Add claim 38 as follows:

38. The semiconductor memory device of claim 30, wherein said data storage circuit comprises a data buffer.

Add claim 39 as follows:

39. The semiconductor memory device of claim 30, wherein said data storage circuit comprises a combination of a sense amplifier and a data input/output buffer.

Add claim 40 as follows:

40. The semiconductor memory device of claim 39, wherein said data storage circuit further includes column select gates.

Add claim 41 as follows:

41. The semiconductor memory device of claim 29, wherein said memory cell array includes NAND memory cells.

Add claim 42 as follows:

42. The semiconductor memory device of claim 29, wherein said memory cell array includes string-connected cells.

Add claim 43 as follows:

43. The semiconductor memory device of claim 29, wherein said memory cell array includes serially connected memory cells.

Add claim 44 as follows:

44. The semiconductor memory device of claim 29, wherein said memory cell array includes serially connected memory cells, wherein reading, erasing, and programming of said memory cells controls the threshold voltages of the memory cells.

Add claim 45 as follows:

45. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of page data state "11", page data state "10", page data state "00", and page data state "01" of data that differ in threshold voltage;

a control circuit which controls a potential on said bit line and that on said word line, wherein

said control circuit operates in such a manner that

in a first read operation, the bit line receives data of a first logical level when the data in said memory element is in either page data state "11" or page data state "10", and receives data a second logical level when the data in said memory element is in either page data state "00" or page data state "01", and

that in a second read operation, the bit line receives data of the first logical level when the data in said memory element is in either page data state "11" or page data state "01", and receives data of the second logical level when the data in said memory element is in either page data state "10" or page data state "00".

Add claim 46 as follows:

46. The nonvolatile semiconductor memory device according to claim 15, wherein

said control circuit judges whether the data in said memory element is in either page data state "10" or below or page data state "00" or above in said first read operation and judges not only whether the data in said memory element is in either page data state "11" or page data state "10" or above but also whether the data is in either page data state "00" or below or page data state "01" in said second read operation.

Add claim 47 as follows:

47. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of page data state "11", page data state "10", page data state "00", and page data state "01" of data that differ in threshold voltage;

a control circuit which controls a potential on said bit line and that on said word line, wherein

said control circuit operates in such a manner that

in a read operation of one of a first page and a second page of data, the bit line receives data of a first logical level when the data in said memory element is in either page data state "11" or page data state "10", and receives data a second logical level when the data in said memory element is in either page data state "00" or page data state "01", and

that in a read operation of the other of said first page and said second page of data, the bit line receives data of the first logical level when the data in said memory element is in either page data state "11" or page data state "01", and receives data of the second logical level when the data in said memory element is in either page data state "10" or page data state "00".

Add claim 48 as follows:

48. The nonvolatile semiconductor memory device according to claim 15, wherein

said control circuit judges whether the data in said memory element is in either page data state "10" or below or page data state "00" or above in said read operation of said one of said first page and said second page of data and judges not only whether the data in said memory element is in either page data state "11" or page data state "10" or above but also whether the data is in either page data state "00" or below or page data state "01" in said read operation of the other of said first page and said second page of data.